ARQ-LVD001

RAD-HARD 500 Mbps Bus LVDS Quad Driver

FEATURES

- 500.0 Mbps low jitter data path
- 3.3 V power supply
- Low Power Consumption
- 24 mA output driver short circuit (OUT+, OUT−)
- Cold sparing on all pins
- Propagation delay of 2 ns at extreme temperatures
- Radiation tolerant: 300 krad(Si)
- Latch-up free up to 67 MeVcm^2/mg
- ESD tolerance: 8 kV
- Packaging: 16 pin, Ceramic Flat Pack (FP-16).
- Compliant with ANSI TIA/EIA 644a standard (LVDS)
- Space level

DESCRIPTION

ARQUIMEA's ARQ-LVD001 device is a Quad Driver for Low Voltage Differential Signals (LVDS) for low power, high speed operation. Data paths are fully differential output for low noise generation and low pulse width distortion. LVDS enable high speed data transmission for point-to-point or multi-drop interconnects. This device is designed for use as a high speed differential Driver.

The ARQ-LVD001 Quad Driver is a quad CMOS LVDS driver designed high speed operation with low power dissipation. The ARQ-LVD001 utilizes CMOS/TTL input signaling to deliver high speed low voltage differential output signals while consuming minimal power with reduced EMI.
The LVDS outputs can be put into Tri-State by use of the enable pins.

All pins, including CMOS inputs, have Cold Spare capabilities. The pins will be high impedance when VDD is tied to VSS.

APPLICATIONS

The ARQ-LVD001 provides the basic LVDS driver function. The device operates as a Quad Driver LVDS, generating a LVDS signal from a CMOS/TTL input.

The intended application of these devices and signaling technique is for both space-wire point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media. The transmission media may be printed-circuit board traces, backplanes, or cables.

RADIATION HARDENING

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
TID	300	-	-	krad	
SEL	67	-	-	MeV·cm^2/mg	
SEE performance	10^{-13}	-	-	Err/Bit/day	For a GEO orbit (TBC)

More information about radiation hardening features and radiation test conditions is available under request.

AVAILABLE OPTIONS

PRODUCT	Quality Level	PACKAGE	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA
ARQ-LVD001	S - Space	16-FP	-55°C to 125°C	ARQ-LVD001S-01	50-piece tray

INDEX

GLOSSARY

BER	*Bit Error Ratio*
CMRR	*Common Mode Rejection Ratio*
CQFP	*Ceramic Quad Flat Pack*
ESD	*Electrostatic Discharge*
GEO	*Geostationary Earth Orbit*
IC	*Integrated Circuit*
I/O	*Input/Output*
LET	*Linear Energy Transfer*
LVDS	*Low Voltage Differential Signaling*
LVTTL	*Low Voltage Transistor-Transistor Logic*
PSRR	*Power Supply Rejection Ratio*
RL	*Load Resistor*
SEE	*Single Event Effect*
SEL	*Single Event Latch-up*
TID	*Total Ionizing Dose*
tf	*Fall Time*
tr	*Rise Time*
TTL	*Transistor-Transistor Logic*
VCM	*Common-mode voltage*
VID	*Differential Input Voltage*
VOS	*Offset voltage*
VT	*Differential output voltage*

OVERVIEW

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The intended application of these devices and signaling technique is for both point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media.

BLOCK DIAGRAM

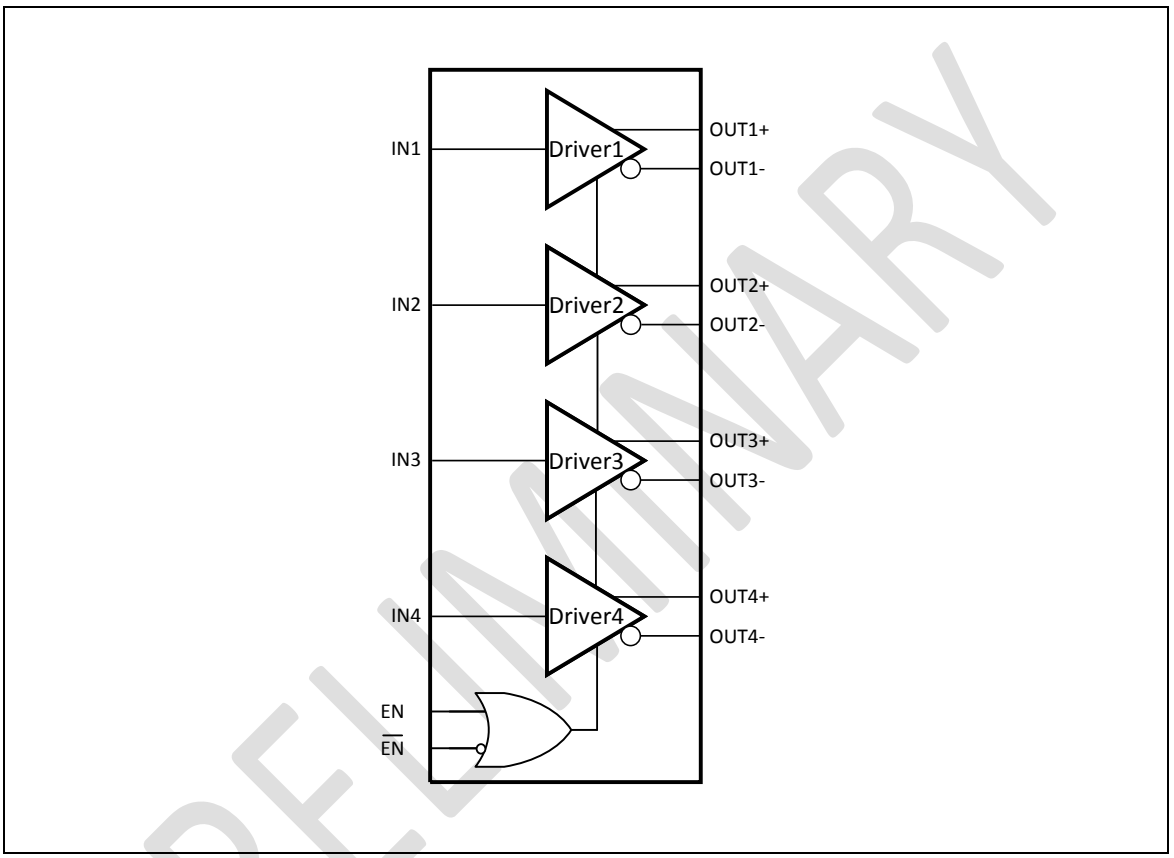

Figure 1: Block diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	VALUE
V_{DD}	DC supply voltage	-0.5 V to 4.6 V
V_I	TTL/CMOS Input Voltage	-0.5 V to 6 V
T_{STG}	Storage temperature	-65°C to +150°C
T_J	Maximum junction temperature	+175°C
Tc	Maximum Case temperature	+125°C
ESD	ESD Last Passing Voltage – HBM	8 kV
P_D	Power dissipation	100 mW (TBC)

Table 1: Absolute Maximum Rating

Note: Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE
V_{DD}	Power supply voltage	3.0 V to 3.6 V
V_{IN}	DC input voltage, logic inputs (EN or EN/)	0 V to 5 V
T_C	Case temperature range	-55°C to +125°C

Table 2: Recommended Operating Conditions

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for VDD = 3.3V±0.3V, -55°C < TC < +125°C

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
TTL/CMOS DC SPECIFICATIONS (EN, ENn and IN)					
V_{IH}	High-level input voltage		2.0	5	V
V_{IL}	Low-level input voltage		-0.3	0.8	V
I_{IH}	High-level input current	V_{IN} = 3.6 V; V_{DD} = 3.6 V	-10	+10	µA
I_{IL}	Low-level input current	V_{IN} = 0 V; V_{DD} = 3.6 V	-10	+10	µA
I_{CS}	Cold Spare Leakage current	V_{IN} = 3.6 V, V_{DD} = V_{SS}	-3,6	+3,6	µA
LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)					
V_{OD}	Differential Output Voltage	R_L = 100 Ω	247	453	mV
ΔV_{OD}	Change in V_{OD} between complementary output states	R_L = 100 Ω		10	mV
V_{OS}	Offset Voltage	R_L = 100 Ω $V_{OS} = \frac{V_{OH}+V_{OL}}{2}$	1.125	1.375	V
ΔV_{OS}	Change in V_{OS} between complementary output states	R_L = 100 Ω		50	mV
ΔV_{OSB}	Imbalance of Differential Offset Voltage during Voltage transition	R_L = 100Ω, C_L = 1 pf		150	mV
I_{OZ}	Output Tri-State Current	Tri-State output (channel disabled), V_{DD} = 3.6 V, V_{OUT} = V_{DD} or GND	-20	+20	µA
I_{CSOUT}	Cold Sparing Leakage Current	V_{OUT} = 3.6V, V_{DD} = V_{SS}	-20	+20	µA
I_{OS}	Output Short Circuit Current	V_{OUT+}=V_{OUT-}=0V		-24	mA
		V_{OUT+}=V_{OUT-}		-12	mA
SUPPLY CURRENT					
I_{CLL}	Total Supply Current	R_L = 100 Ω, C_L = 1 pf; ENn = V_{SS}, EN = V_{DD}, V_{DD} = 3.6 V, Fq = 250 MHz		30 (TBC)	mA
I_{CCZ}	Tri-State Supply Current	ENn = V_{DD}, EN = V_{SS}, V_{DD} = 3.6 V		5	mA

Table 3: DC Electrical Characteristics

AC SWITCHING CHARACTERISTICS

Unless otherwise stated, these specifications apply for VDD = 3.3 V ± 0.3 V, TA = -55°C to +125°C.

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
t_{PHZ}	Disable Time (Active to Tri-State) High to Z	R_L = 100 Ω, C_L = 10 pf		4.5	ns
t_{PLZ}	Disable Time (Active to Tri-State) Low to Z	R_L = 100 Ω, C_L = 10 pf		4.5	ns
t_{PZH}	Enable Time (Tri-State to Active) Z to High	R_L = 100 Ω, C_L = 10 pf		TBD	ns
t_{PZL}	Enable Time (Tri-State to Active) Z to Low	R_L = 100 Ω, C_L = 10 pf		TBD	ns
t_{LHT}	Input/Output Low-to-High Transition Time, 20% to 80%	R_L = 100 Ω, C_L = 1 pf	210	300	ps
t_{HLT}	Input/Output High-to-Low Transition Time, 80% to 20%	R_L = 100 Ω, C_L = 1 pf	210	300	ps
t_{PLHD}	Propagation Low to High Delay	R_L = 100 Ω, C_L = 1 pf		1.5	ns
t_{PHLD}	Propagation High to Low Delay	R_L = 100 Ω, C_L = 1 pf		1.5	ns
T_{SKEW}	Differential Skew t_{PHLD} - t_{PLHD}			200	ps
T_{CCS}	Output Channel-to-Channel Skew			TBD	ps

Table 4: AC Electrical Characteristics

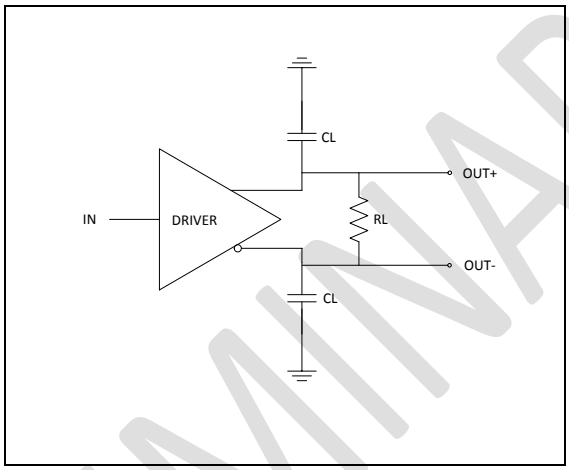

Figure 2: LVDS Output load

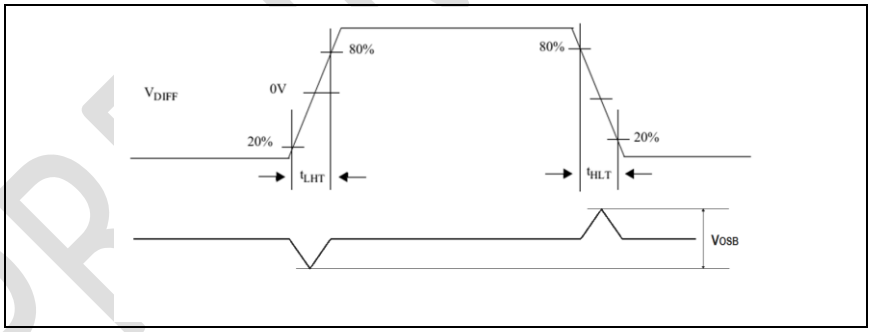

Figure 3: LVDS Output Transition time

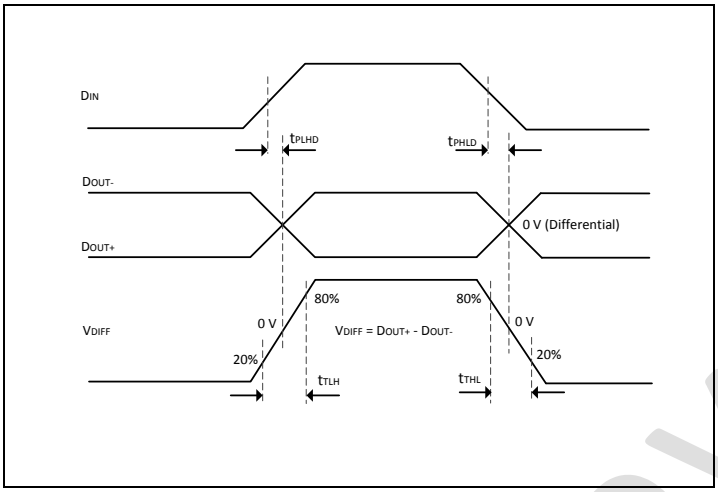

Figure 4: LVDS Propagation delay L->H and H->L and transition time

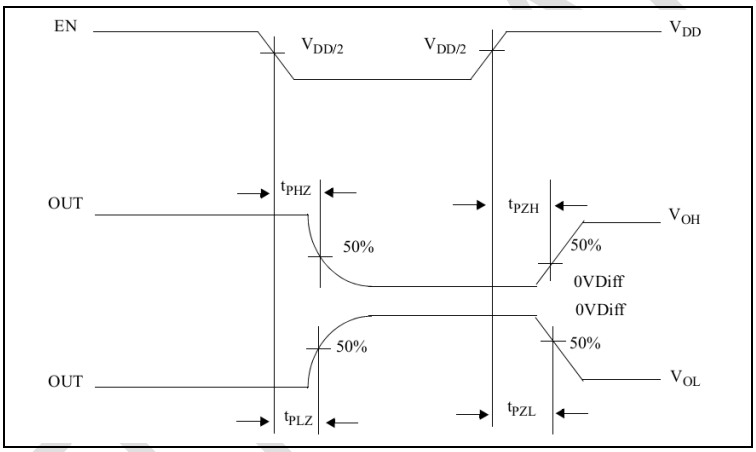

Figure 5: Output active to TRISTATE and TRISTATE to active

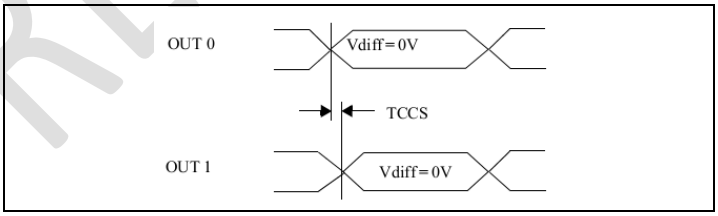

Figure 6: Output channel to channel skew

APPLICATIONS INFORMATION

Transmission media:

The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics.)

The signal path should be matched in length to avoid any skew in differential lines or between channels.

PCB layout and Power System Bypass:

Circuit board layout and stack-up for the ARQ-LVD001 should be designed to provide noise-free power to the device.

Good layout practice also will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. A 0.25 Ω resistor is recommended in the power supply line path. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use value of 0.1 µF. Tantalum capacitors may be 2.2 µF. Voltage rating for tantalum capacitors should be at least 5x the power supply voltage being used. It is recommended practice to use two vias at each power pin of the ARQ-LVD001, as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance and extends the effective frequency range of the bypass components.

The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation, as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity in signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

PINOUT DESCRIPTION

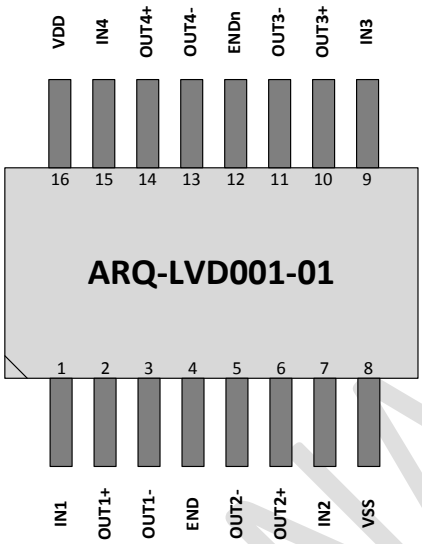

Figure 7: Pinout diagram

Pin Nº	Name	Type	Description
1	IN1	Input	CMOS/TTL input, channel 1
2	OUT1+	Output	Non-Inverting LVDS output, cannel 1
3	OUT1-	Output	Inverting LVDS output, cannel 1
4	END	Input	Logic enable for the LVDS
5	OUT2-	Output	Inverting LVDS output, cannel 2
6	OUT2+	Output	Non-Inverting LVDS output, cannel 2
7	IN2	Input	CMOS/TTL input, channel 2
8	VSS	Power	Ground
9	IN3	Input	CMOS/TTL input, channel 3
10	OUT3+	Output	Non-Inverting LVDS output, cannel 3
11	OUT3-	Output	Inverting LVDS output, cannel 3
12	ENDn	Input	Logic active low enable for the LVDS
13	OUT4-	Output	Inverting LVDS output, cannel 4
14	OUT4+	Output	Non-Inverting LVDS output, cannel 4
15	IN4	Input	CMOS/TTL input, channel 4
16	VDD	Power	3.3 V Power

Table 5: Pinout description

PACKAGE

FP16 Drawing

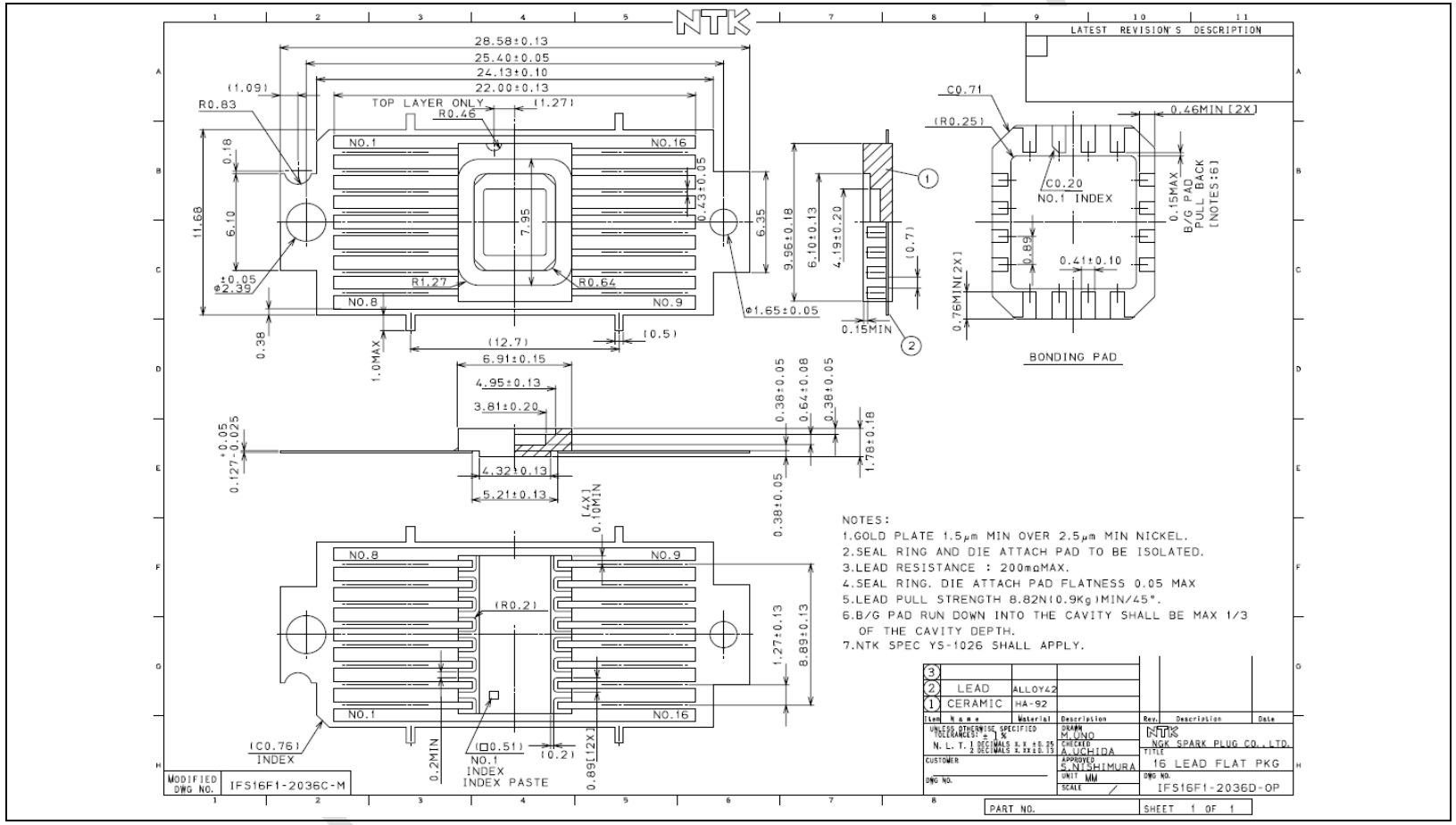

Figure 8: FP-16 Package drawing

QUALITY STANDARDS

ARQUIMEA INGENIERÍA S.L.U. develops its activities under the premises of quality and sustainability, offering efficient, liable and innovative technologies and solutions to its customers.

ARQUIMEA's Quality Management System meets the requirements of ISO 9100:2010 Aerospace Series, and has been audited and certified by the Spanish Association for Standardization and Certification, AENOR.

In order to meet the highest quality and reliability, ARQUIMEA designs and develops its aerospace product line according to military and space standards.

Our space microelectronic devices are available in one or more of the following processes:
- Equivalent to QML 38535 LEVEL Q or Level V*
- Equivalent to ESCC 9000*

For procurement in die form
- In accordance with ECSS-Q-ST-60-05C
- Equivalent to QML 38534 LEVEL H or Level K*

*With Radiation Qualification

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REVISION HISTORY

Date Released	Issue	Section	Changes
04-04-2016	Draft A	All	Initial Release.
23-09-2016	Draft B	ELECTRICAL CHARACTERISTICS	Parameter update after electrical Measurements
		AC SWITCHING CHARACTERISTICS	

Space Technology Partner

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